

Atty. Dkt. No. 025572-0102

**REMARKS**

Applicant respectfully requests reconsideration of the present application in view of the foregoing amendments and in view of the reasons which follow.

**Drawings**

FIG. 9 has been added for clarity. FIG. 9 is a depiction of the optical gate of FIG. 2 formed on the substrate of FIG. 8. The combination of FIG. 2 and FIG. 8 has been well described throughout the specification. Accordingly, no new matter is presented.

**DETAILED ACTION****Claim Rejections – 35 U.S.C. § 103**

In section 8 of the Office action, the Examiner rejected claims 1, 4-10, 11, 13-15, 17-22, 36 and 38-46 under 35 U.S.C. 103(a) as being unpatentable over the patent issued to Utaka et al. in view of the patent issued to Yang.

Also, in section 9 of the Office action, the Examiner rejected claims 31 and 33-35 rejected under 35 U.S.C. 103(a) as being unpatentable over the patent issued to Yang in view of the patent issued to Utaka et al.

Claims 1-22 and claims 31-46 are cancelled without prejudice. New claims 47-78 have been added.

With regard to independent claims, 47, 55, 69, and 69 neither Utaka et al. nor Yang discloses, teaches, suggests, alone or in any proper combination, an optical logic circuit having a substrate and an optical layer overlaying the substrate. The optical layer is formed with a plurality of optical pathways and an interference region. Further, the optical pathways include two optical inputs to the interference region, one optical input providing a constant source of coherent light. The other of the two optical inputs provides a coherent light input which can be selectively turned on and off (conventionally representative of a binary 1 or 0 respectively). The output of the interference region is

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positioned such that an interference line is aligned with the output and therefore wavefronts interfering cause a dark output. Output signals are Boolean logic output signals based on the second optical input signal and the optical output signal exits the interference region output. Utaka et al. teaches a system of optical pathways in which light waves are not coherent in paths I and II, rather the phase of light wave  $P_1$  is modulated by inputs  $P_1$  and  $P_2$ . Yang teaches a mechanical structure having mechanical gates to provide an interference region. However, Yang does not provide that the optical gates are formed over a substrate using an optical layer that overlays the substrate and forms the optical pathways and interference region.

Further, neither Utaka et al. nor Yang teaches, alone or in any proper combination, an optical logic gate for an optical processor that is formed on a substrate and via a patterned optical layer which overlays the substrate. The optical layer includes a plurality of optical conduits formed of the second material where at least two of the optical conduits are configured to receive optical input signals, each of the optical input signals provide coherent light inputs. Again, Utaka et al. does not provide such light inputs to an interference region and Yang does not provide any teaching or suggestion to provide the mechanical gates formed in an optical layer overlaying a substrate.

Accordingly, independent claims 47, 55, 65, and 69 and their dependent claims are not disclosed, taught, or suggested, alone or in any proper combination of Utaka et al. and Yang. Therefore, independent claims 47, 55, 65, and 69 and their respective dependent claims are therefore allowable.

After amending the claims as set forth above, claims 47-78 are now pending in this application.

Applicant believes that the present application is now in condition for allowance. Favorable reconsideration of the application as amended is respectfully requested.

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The Examiner is invited to contact the undersigned by telephone if it is felt that a telephone interview would advance the prosecution of the present application.

Respectfully submitted,

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